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1 Classification and performance evaluation of instruction buffering techniques

Lizyamma Kurian, Paul T. Hulina, Lee D. Coraor, Dhamir N. Mannai

April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture**, Volume 19 Issue 3

Full text available: pdf(940.03 KB) Additional Information: full citation, references, citings, index terms

2 Session 1: Safe memory reclamation for dynamic lock-free objects using atomic reads and writes

Maged M. Michael

July 2002 **Proceedings of the twenty-first annual symposium on Principles of distributed computing**

Full text available: pdf(1.13 MB) Additional Information: full citation, abstract, references, citings

A major obstacle to the wide use of lock-free data structures, despite their many performance and reliability advantages, is the absence of a practical lock-free method for reclaiming the memory of dynamic nodes removed from dynamic lock-free objects for arbitrary reuse.The only prior lock-free memory reclamation method depends on the DCAS atomic primitive, which is not supported on any current processor architecture. Other memory management methods are blocking, require special operating system ...

3 Pipelined memory shared buffer for VLSI switches

Manolis Katevenis, Panagiota Vatsolaki, Aristides Efthymiou

October 1995 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication**, Volume 25 Issue 4

Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

Switch chips are building blocks for computer and communication systems. Switches need internal buffering, because of output contention; shared buffering is known to perform better than multiple input queues or buffers, and the VLSI implementation of the former is *not* more expensive than the latter. We present a new organization for a shared buffer with its associated switching and cut-through functions. It is simpler and smaller than wide or interleaved organizations, and it is particula ...

Keywords: crossbar switch, gigabit VLSI switch buffer, input queueing, multiport buffer, pipelined memory, shared buffering